

**AMENDMENTS TO THE CLAIMS**

1. (currently amended) An NROM memory transistor comprising:
  - a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;
  - a nanolaminate gate dielectric formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric comprising a an oxide-nitride-high-k dielectric composition of one of ~~atomic layer deposition (ALD) Lanthanide (Pr, Ne, Sm, Gd, and Dy) Oxide—ALD ZrO<sub>2</sub>—ALD Lanthanide Oxide, ALD Lanthanide Oxide—ALD HfO<sub>2</sub>—ALD Lanthanide Oxide, or ALD Lanthanide Oxide—evaporated HfO<sub>2</sub>—ALD Lanthanide Oxide~~ oxide – nitride – Al<sub>2</sub>O<sub>3</sub>, oxide – nitride – HfO<sub>2</sub>, or oxide – nitride – ZrO<sub>2</sub>; and
  - a control gate formed on top of the gate dielectric.
- 2 – 5 (canceled)
6. (currently amended) An NROM memory transistor comprising:
  - a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;
  - a composite gate insulator layer formed on top of the substrate and substantially between the plurality of source/drain regions, the gate insulator comprises a composition of high-k – high-k – high-k dielectric layers of one of: ~~one of atomic layer deposition (ALD) Lanthanide (Pr, Ne, Sm, Gd, and Dy) Oxide—ALD ZrO<sub>2</sub>—ALD Lanthanide Oxide, ALD Lanthanide Oxide—ALD HfO<sub>2</sub>—ALD Lanthanide Oxide, or ALD Lanthanide Oxide—evaporated HfO<sub>2</sub>—ALD Lanthanide Oxide~~ HfO<sub>2</sub> – Ta<sub>2</sub>O<sub>5</sub> – HfO<sub>2</sub> or HfO<sub>2</sub> – ZrO<sub>2</sub> – HfO<sub>2</sub>; and
  - a control gate formed on top of the gate insulator layer.
7. (canceled)

8. (original) The transistor of claim 6 wherein the plurality of source/drain regions are comprised of an n+ type doped silicon.

9. (original) The transistor of claim 6 wherein the control gate is a polysilicon material.

10. (original) The transistor of claim 6 wherein the substrate is comprised of a p+ type silicon material.

11 – 14 (canceled)

15. (currently amended) An electronic system comprising:  
a processor that generates control signals; and  
a memory array coupled to the processor, the array comprising a plurality of NROM memory cells, each NROM memory cell comprising:  
a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;  
a nanolaminate gate dielectric formed on top of the substrate substantially between each pair of the plurality of source/drain regions, the gate dielectric comprises a composition of high-k – high-k – high-k dielectric layers of one of: one of atomic layer deposition (ALD) Lanthanide (Pr, Ne, Sm, Gd, and Dy) Oxide – ALD ZrO<sub>2</sub> – ALD Lanthanide Oxide, ALD Lanthanide Oxide – ALD HfO<sub>2</sub> – ALD Lanthanide Oxide, or ALD Lanthanide Oxide – evaporated HfO<sub>2</sub> – ALD Lanthanide Oxide atomic layer deposited (ALD) HfO<sub>2</sub> – ALD Ta<sub>2</sub>O<sub>5</sub> – ALD HfO<sub>2</sub> or ALD HfO<sub>2</sub> – ALD ZrO<sub>2</sub> – ALD HfO<sub>2</sub>; and  
a control gate formed on top of the oxide insulator.

16-34 (canceled)